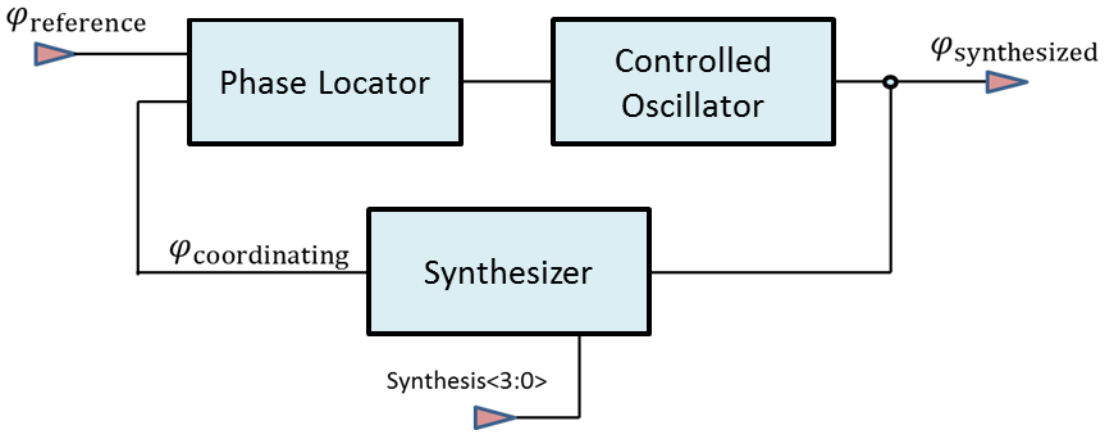
Ideal Frequency Synthesizer

Gain ICs

ILS_3G375M

An instantaneous loop (iL) synthesizer, designed with an instantaneous loop or ideal Phase Locked Loop (PLL), achieves breakthrough advances in phase tracking with high loop gain. Salient are roughly a millions times faster tracking bandwidth, low nanosecond range lock times versus typical millisecond or higher range, and orders of magnitude reduction in jitter over typical tracking.

- Output from 300 MHz to 3 GHz
- Near-ideal phase coherence
- Orders of magnitude reduction in jitter, or phase noise
- Fractional-n synthesis and unity synthesis

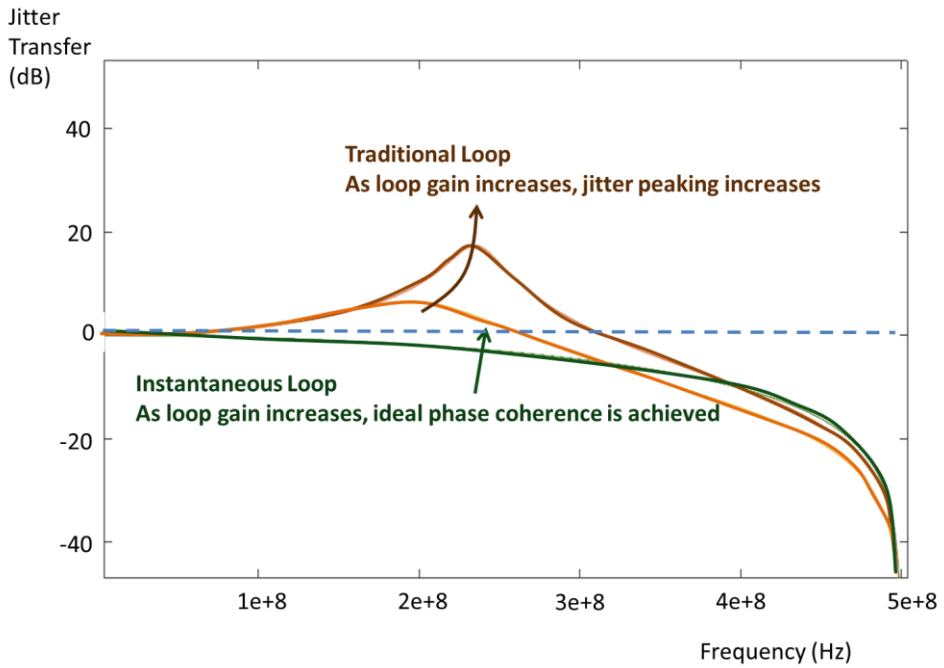


Interface

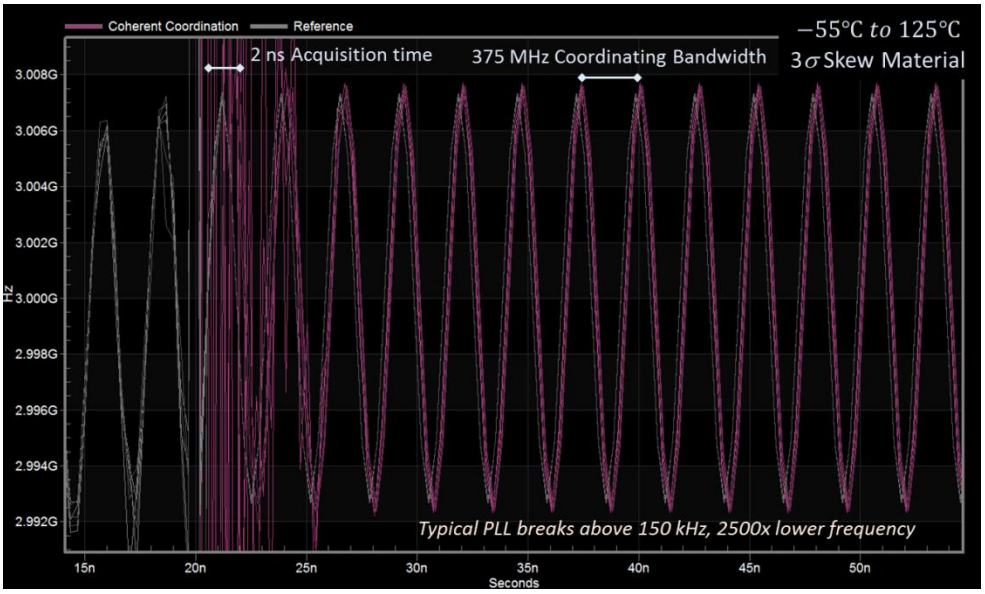
Interface	Direction	Description
$\varphi_{\text{reference}}$	in	Input or reference clock
Synthesis<3:0>	in	Program synthesis ratio (low frequency)
$\varphi_{\text{synthesized}}$	out	iL output clock

Performance Specifications

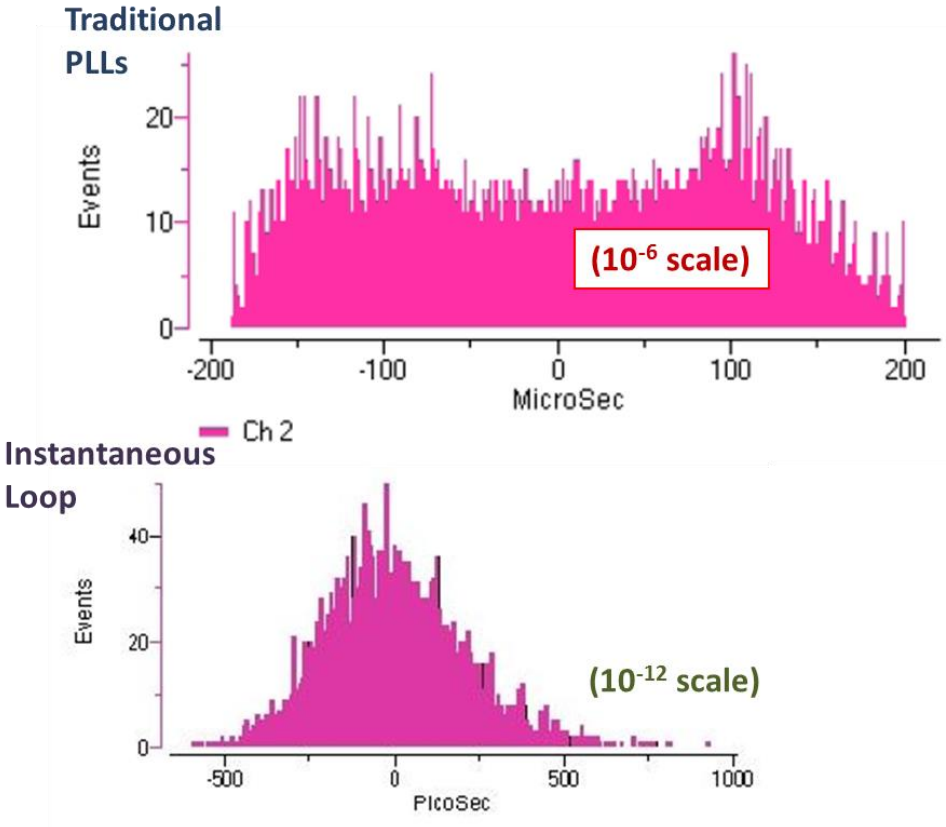
Parameter	**Specification (Worst case or range across -55 °C to 125 °C and 3σ material skew)**
Coordinating (Tracking) bandwidth[1, 2]	Frequency/2 (1.5 GHz at 3 GHz reference)
Jitter peaking and accumulation over coordinating (Tracking) bandwidth[3]	Less than 0.02%
Phase Noise (3 GHz Output)[4]	100x decrease over typical phase tracking
Acquisition (startup/settle/lock) time	8 ns (~1,000,000x faster than typical PLLs)
Output frequency range	300 MHz to 3 GHz
Frequency Aliasing	None, intrinsic to iL design
Voltage	1.2 V
Power consumption	<4 mA



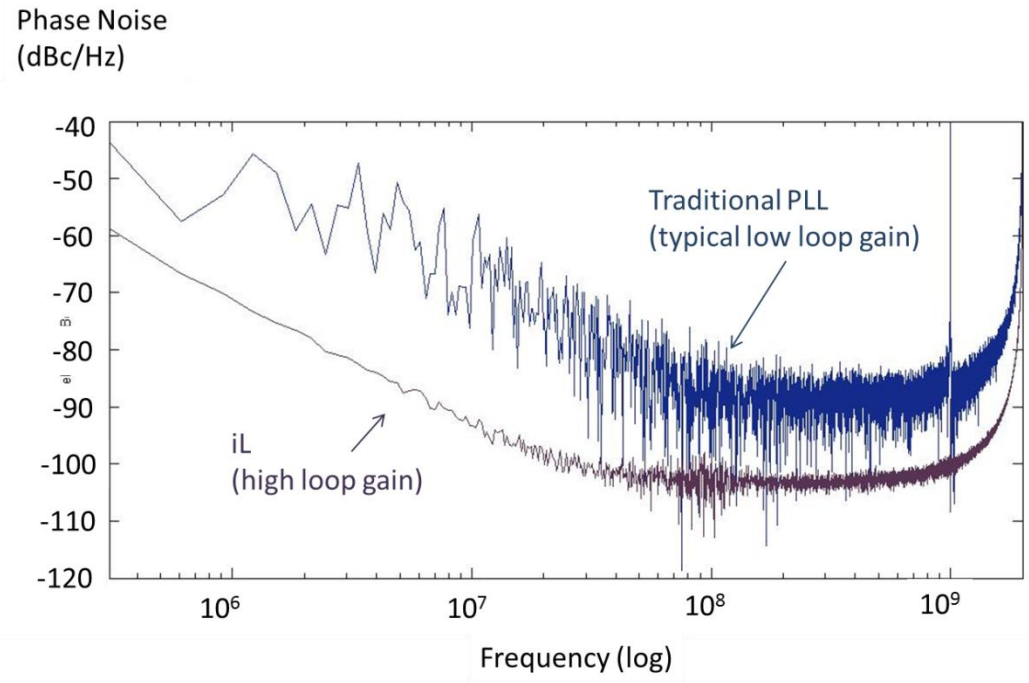
[1] Tracking bandwidth increases as tracking accuracy, loop gain, increases with iL.



[2] Time domain showing ideal phase coherence of instantaneous loop.

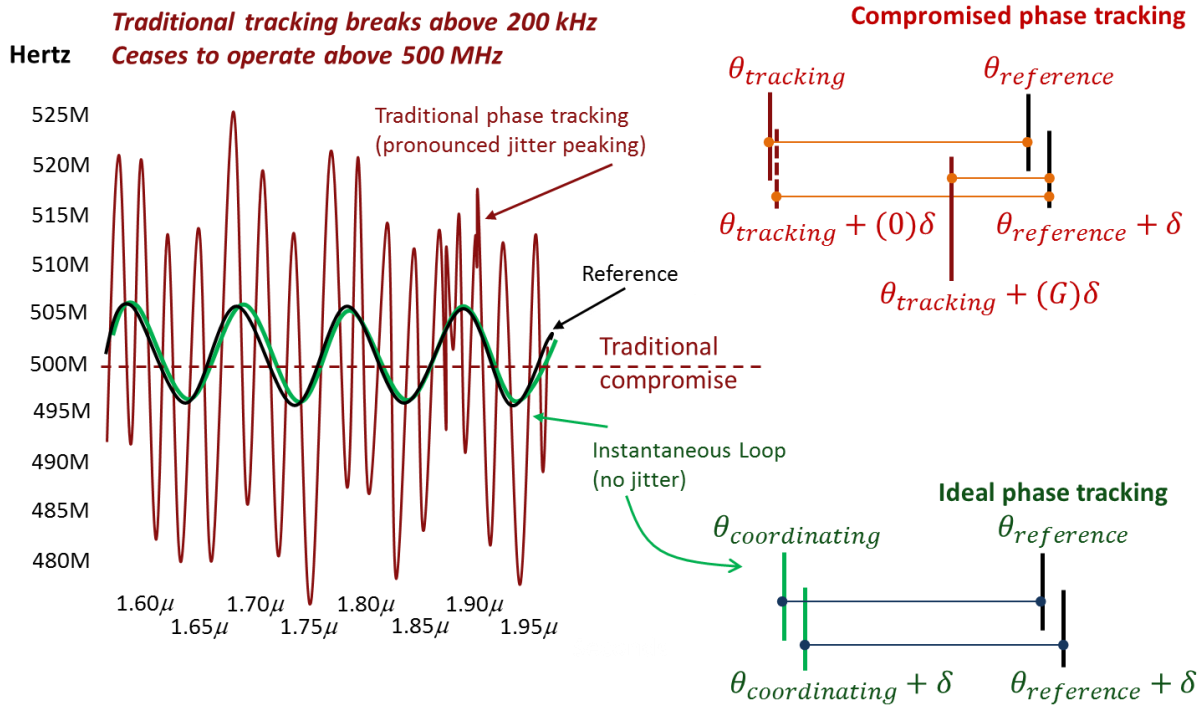


[3] Silicon measurements show 400,000 times less jitter for instantaneous loop with same noise profile, and all else being equal. Instantaneous loop eliminates jitter peaking and jitter accumulation.



[4] Phase noise measured with same non-optimized loop elements other than phase detection for both PLLs and under non-ideal operating conditions, showing instantaneous loop 100 times lower than that of typical phase tracking.

Instantaneous Loop versus Far Less Ideal Traditional PLLs



Synthesis Jitter Reduction