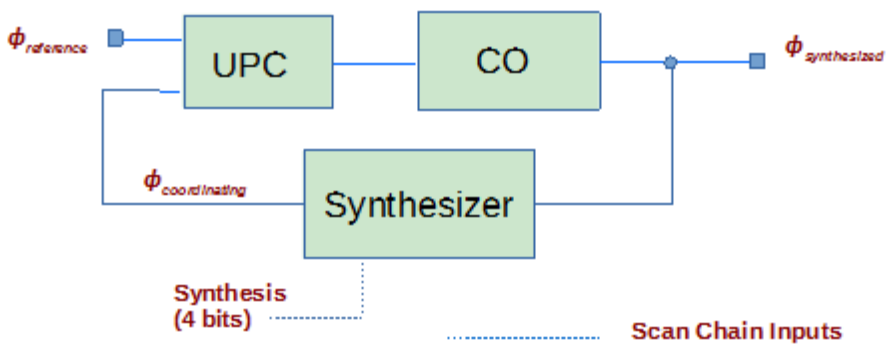
IL3G375MLP

A low power instantaneous loop (IL), an ideal phase locked loop (PLL) with instantaneous coherence, IP layout block designed in 55 nm process. Salient advances of IL over PLLs, with typical phase tracking, are roughly a millions times faster tracking bandwidth, or ultra phase coordination (UPC). Integrated circuits using IL clocking can now power on in low nanoseconds versus typical milliseconds or longer. With hundred times lower phase noise, integrated circuits can operate more reliably with less jitter, lower power, at higher frequencies.

- Phase coordination (tracking) to 375 MHz
    - Reaching 10,000 times wider than typical PLLs
- Output from 2.5 GHz to 3.5 GHz
- Phase noise reduction of 100 times (track low phase noise of crystal)
- Fractional-n synthesis and unity synthesis

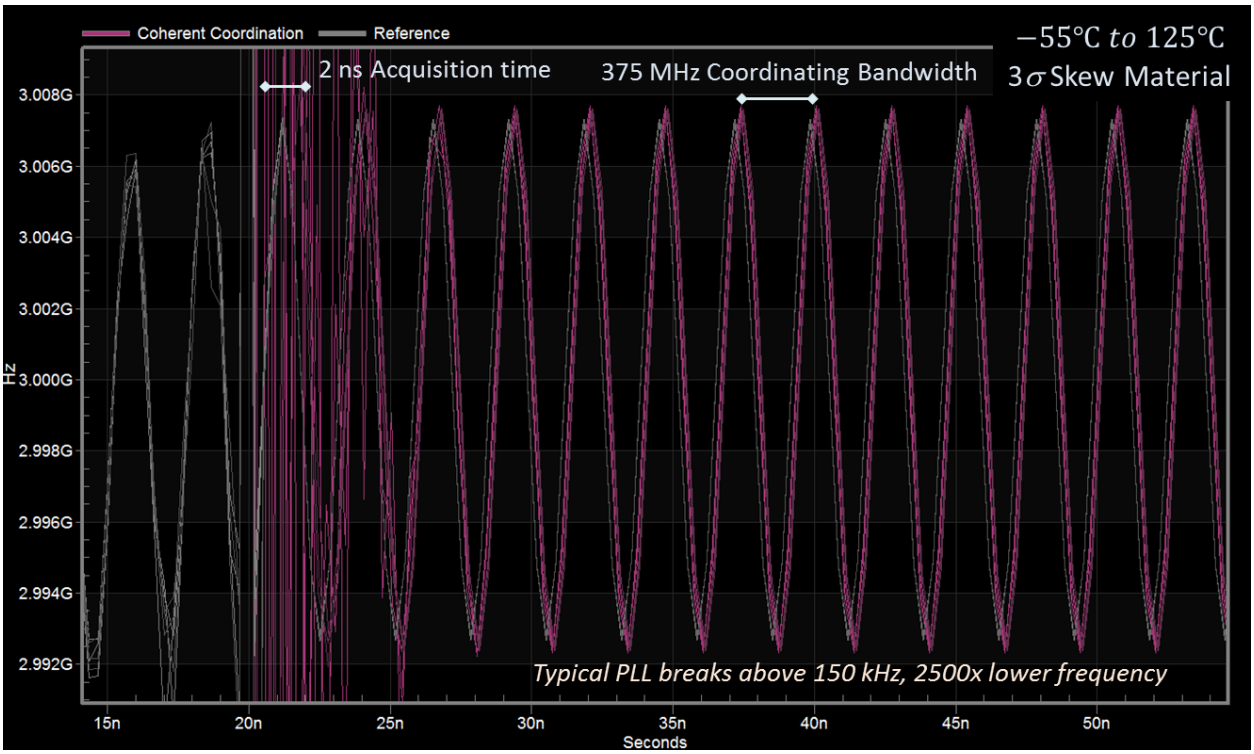


Interface Ports

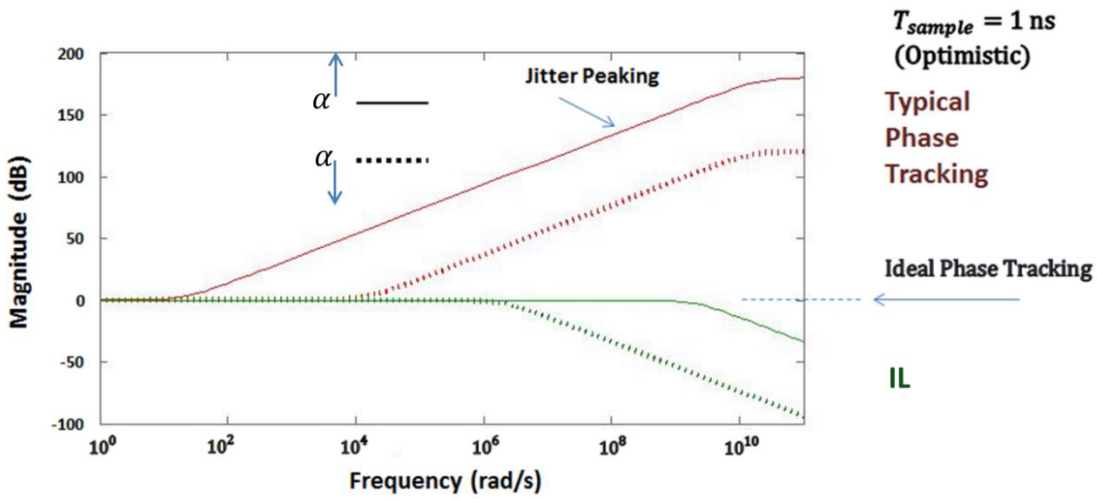
Interface	*Direction/serial*	*Description*
$\phi_{reference}$	In	Input or reference clock
Synthesis<3:0>	In/serial	Set frequency synthesis ratio
$\phi_{synthesized}$	Out	Synthesized output clock

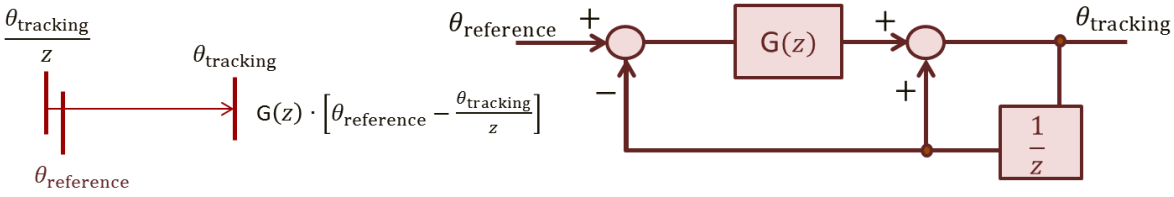
Performance Specifications (-55 °C to 125 °C, 3 σ skew material)

Parameter	*Instantaneous Loop*	*Typical PLL*	*IL Improvement*
Reference Frequency (GHz)	2.5 to 3.5	2.5 to 3.5	
Coordinating/tracking bandwidth[1] (kHz)	375,000 (1/8th $f_{reference}$)	150	2500x
Acquisition, startup (lock/settle) time[1] (s)	$2 \cdot 10^{-9}$	$> 2 \cdot 10^{-3}$	$> 10^{6}$
Jitter peaking/accumulation over tracking bandwidth[2] (time interval error, TIE, plus Rj and Dj period jitter over many cycles)	0.02%	>1%	50x
Phase Noise[3]	N_o	$100 \cdot N_o$	100x
Frequency aliasing effects (harmonic distortion)	$0 \cdot P_{transmit}$ all harmonics, intrinsic to IL	$0.1 \cdot P_{transmit}$ for 2nd and 3rd harmonic	∞
P/N Differential Skew, across skew corners (ps)	7		
tr/tf (20%-80%) (ps)	80		
Hold-in Range (GHz)	2.7		
Supply (V)	1.2	1.2	
Power Static and Dynamic (mW)[4]	2.5 to 2.9		
Indirect System Power (mW)[5] $P_{System} = \propto \cdot P_{Communication} + \beta \cdot P_{Logic}$ $P_x = C \cdot V \cdot SR \cdot N_{Drivers}$	$P_{System_{Drivers}}$	$\sim 7 \cdot P_{System_{Drivers}}$	7x
Startup Energy (joules)	$2 \cdot 10^{-9} P_{System}$	$2 \cdot 10^{-3} P_{System}$	$> 10^{6}$
Die area (um)[2]	180		



[1]IL enables wide coordinating bandwidth and instantaneous acquisition.





$$\theta_{\text{tracking}} = \frac{zG(z)}{G(z)-(1-z)}\,\theta_{\text{reference}}$$

$$G(z) = l\frac{z+1}{z-\alpha} \qquad l = \frac{\beta(\alpha-1)}{2}$$

$$\boldsymbol{\theta_{tracking} = \frac{lz(z+1)}{z^2+(l-\alpha-1)z+\alpha+l}\,\theta_{reference}}$$

PLL, conflict

$as\ \alpha \to \infty$

$\theta_{\text{tracking}}' = z\,\theta_{\text{reference}}'$ (jitter peaking)

$as\ \alpha \to 0$

$\theta_{tracking}' = 0$ (not tracking reference)

Jitter amplification, jitter peaking, denoted by damped oscillation transform

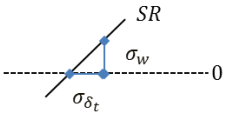
"It has been widely known that the traditional PLL inherently has jitter peaking that cannot be eliminated."

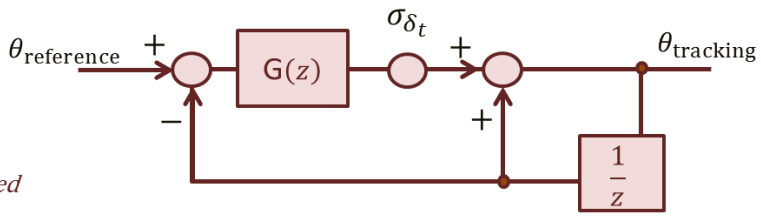
M. Lee, et. Al., "Jitter Transfer Characteristics of Delay-locked Loops—Theories and Design Techniques," *IEEE J. of Solid-state Circuits*, **Vol. 38, NO. 4**, pp. 614-621, Apr. **2003**.

iL, no conflict

$as\ \alpha \to \infty$

$\theta_{\text{tracking}}' = \theta_{\text{reference}}'$ *(no jitter peaking)*





Gaussian Noise, Device and Supply Induced

$$\sigma_w = \frac{(kT)^{\frac{1}{2}}}{\lambda}\left(\frac{K'\frac{W}{L}}{I_D{}^3}\right)^{\frac{1}{4}} + \sigma_{supply} + \sigma$$

$$\sigma_{\delta_t} = \frac{C}{I_D}\left(\frac{(kT)^{\frac{1}{2}}}{\lambda}\left(\frac{K'\frac{W}{L}}{I_D{}^3}\right)^{\frac{1}{4}} + \sigma_{supply} + \sigma\right)$$

Damped oscillation of noise, tracking noise more than reference

$$\boldsymbol{\theta_{tracking}} = \frac{\boldsymbol{z}}{\boldsymbol{z^2 + (\alpha - 2)z + 1}}\left(\sigma_{\delta_t}(\boldsymbol{z-1})\right)$$

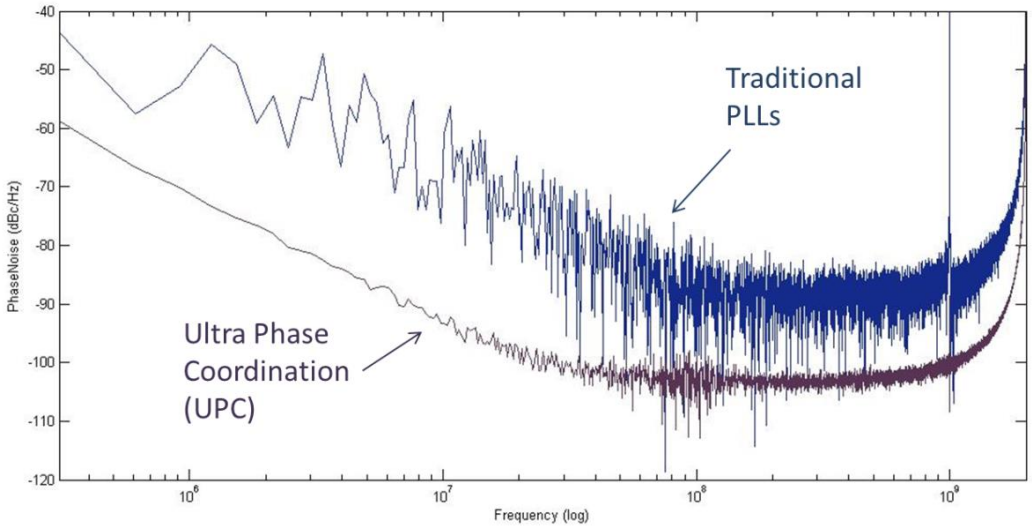
Jitter accumulation, output jitter caused by time varying phase shifts from device and power supply induced noise which accumulate throughout the loop (jitter accumulation inversely proportional to loop gain)

iL

$as\ \alpha \to \infty$

$\theta_{\text{tracking}} \approx \theta_{\text{reference}}$ *(negligible jitter accumulation)*

[2]Significantly lower jitter peaking and jitter accumulation due to UPC of IL across wider coordinating bandwidth (Reduced TIE and periodic jitter across multiple cycles).



[3]Phase noise is significantly reduced via IL, given same VCO used in both.

[4]Transistor areas for IL, and corresponding power, can be safely reduced using Monte Carlo full loop simulations while maintaining loop stability, which cannot be achieved with PLL designs owing to prohibitive acquisition times.

[5]Owing to significantly lower jitter of IL, the slew rates of drivers can be kept at lower slew rates (SR), thus substantially reducing system power proportional to the number of drivers.